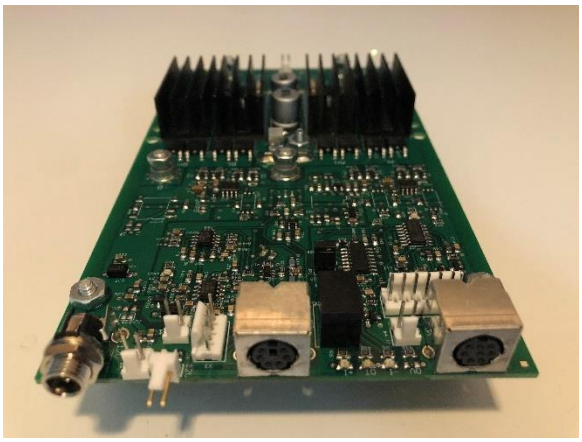
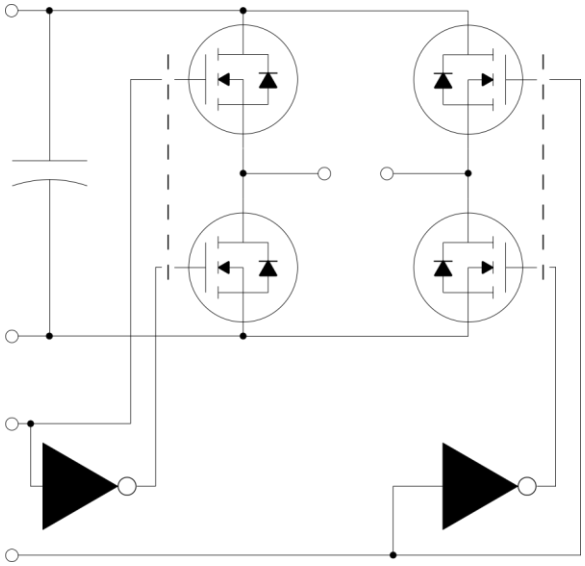
Description:

The SPI-DCI-35V-50A-NI-NF-1 is a MOSFET based H-Bridge assembly that includes monitors, protection, cooling, and a straight-forward interface all on a compact and easily mounted PCB, allowing an engineer or hobbyist to conveniently and cost-effectively focus on developing the controls for his or her application rather than the power electronics. System features include:



- Effective passive cooling
- Temperature, DC bus voltage, and output current monitors
- Over-temperature, over-voltage, over-current, and short circuit protection
- Integrated dead-time insertion
- Integrated free-wheeling diodes
- Integrated 1320uF DC bus capacitor bank
- Direct control of the switch pairs in each phase
- Wide switching range from DC to 200kHz



The H-bridge can be used as a buck or boost converter, inverter, or rectifier enabling applications such as a brushed DC motor drive, single-phase AC motor drive, DC supply, LED drive, PWM rectifier, class D amplifier, or Tesla Coil drive, among countless other power conversion applications.

Absolute Maximum Ratings

Parameter		Max	Unit
DC Bus Voltage		50	V
Output Current		50	A
Junction Temperature		150	°C
Switching Frequency		200	kHz
Power	T_a 25°C	875	W
Input Signal Level		5.5	V

Typical Operating Values, T_a = 25°C

General

Parameter		Min	Typ	Max	Unit
DC Bus Voltage		12	36	50	V
Continuous Output Current			20	25	A_{rms}
Heatsink Temperature				75	°C
Switching Frequency			20	200	kHz
DC Bus Capacitance		1060	1320	1580	µF
Input Signal Level		2.8	5	5.5	V

Control Signal Ratings

Parameter		Min	Typ	Max	Unit
Input Supply Voltage		8	12	13	V
Input Supply Current			0.01	0.25	A
Signal High Threshold		2.7	2.8	2.9	V
Signal Low Threshold		1.8	1.9	2.0	V
Signal Input Impedances		99	100	101	kΩ
Signal Input Filter Corners			1.25		MHz
Monitor Voltages		0		5	V
Voltage Monitor 3dB Bandwidth			150		Hz
Current Monitor 3dB Bandwidth			40		kHz
Auxiliary Supply Voltage			5		V
Auxiliary Supply Current				500	mA

Monitors and Protection

Parameter		Value	Unit
DC Bus Voltage Monitor		12.5	V/V
DC Bus Over-Voltage		45	V
Phase A Current Monitor		33.3	A/V
Phase A Over-Current		50	A
Over-Temperature	See table xxx for relationship	55	°C

Switching Characteristics

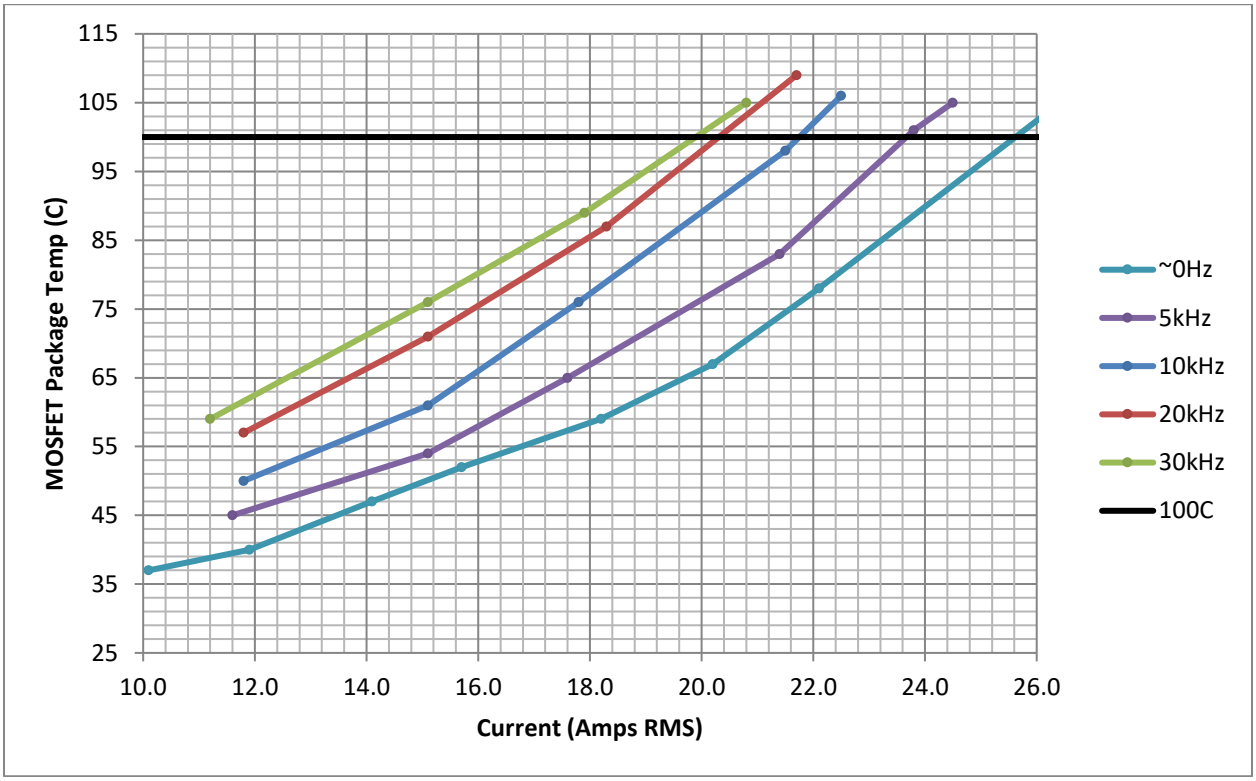
Parameter		Min	Typ	Max	Unit
Dead-Time		470	520	570	ns
Propagation Delay					ns
Rise Time		2000			ns
Fall Time		200			ns

Temperature Sensor Monitor Values

Monitor Voltage (V)		Temperature (°C)
4.27		35
3.66		40
3.20		45
2.80		50
2.49		55
2.24		60
2.04		65
1.88		70
1.74		75
1.63		80
1.54		85
1.46		90

Operation Curves Under Inductive Switching

MOSFET Package Temperature for Selected Switching Frequencies in kHz
Ambient Temperature 25°C, DC Bus 36V



Connections and Pinouts

The SPI-DCI-35V-50A-NI-NF-1 features standard, shielded miniDIN connectors, and polarized male headers in parallel, to control and monitor the power switches. Additionally, a male header connected to the cable shield is provided as well as headers for the supply input. The H-bridge connections are made using threaded M4 studs, preferably through spade or ring terminals.

In the event one of the four fault conditions is triggered, the inverter MOSFETs will be disabled and the LED corresponding to the fault will light up on the edge of the PCB. Those faults and their LED colors are depicted above along with the connectors and their pin numbers.

Connectors

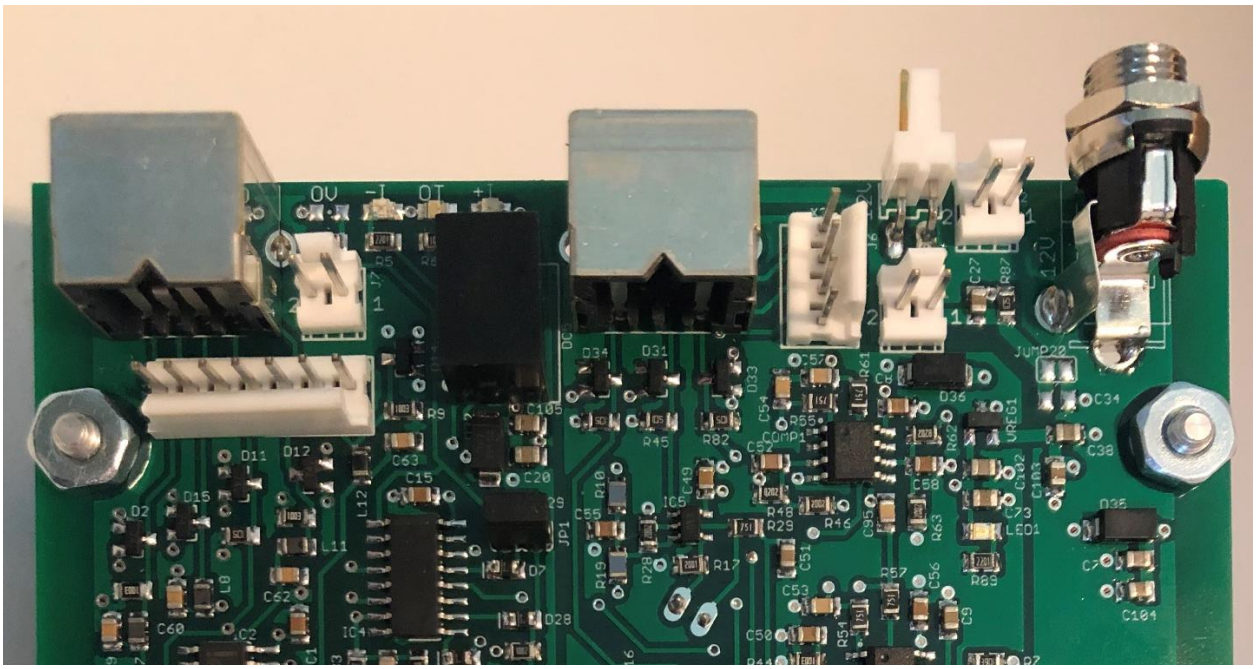
Description		Connector	Specification
Control Signals		miniDIN	6 Pin, Female
Monitor Signals		miniDIN	8 Pin, Female
Low Voltage Supply		Barrel Jack	ID 2.5mm, OD 5.5mm
DC+, DC-, A, and B		Screw Terminal	M4

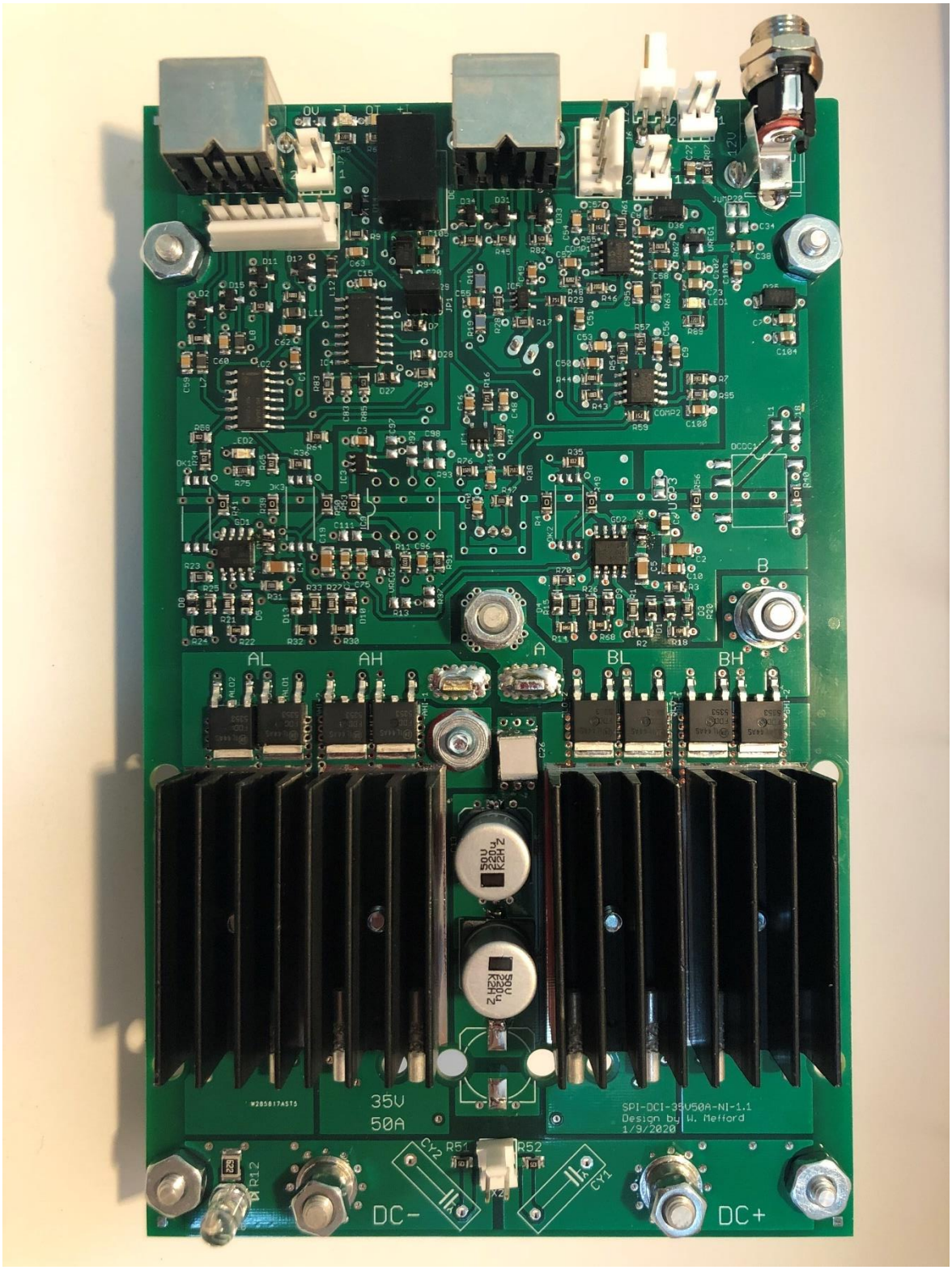
miniDIN, 6 Pin

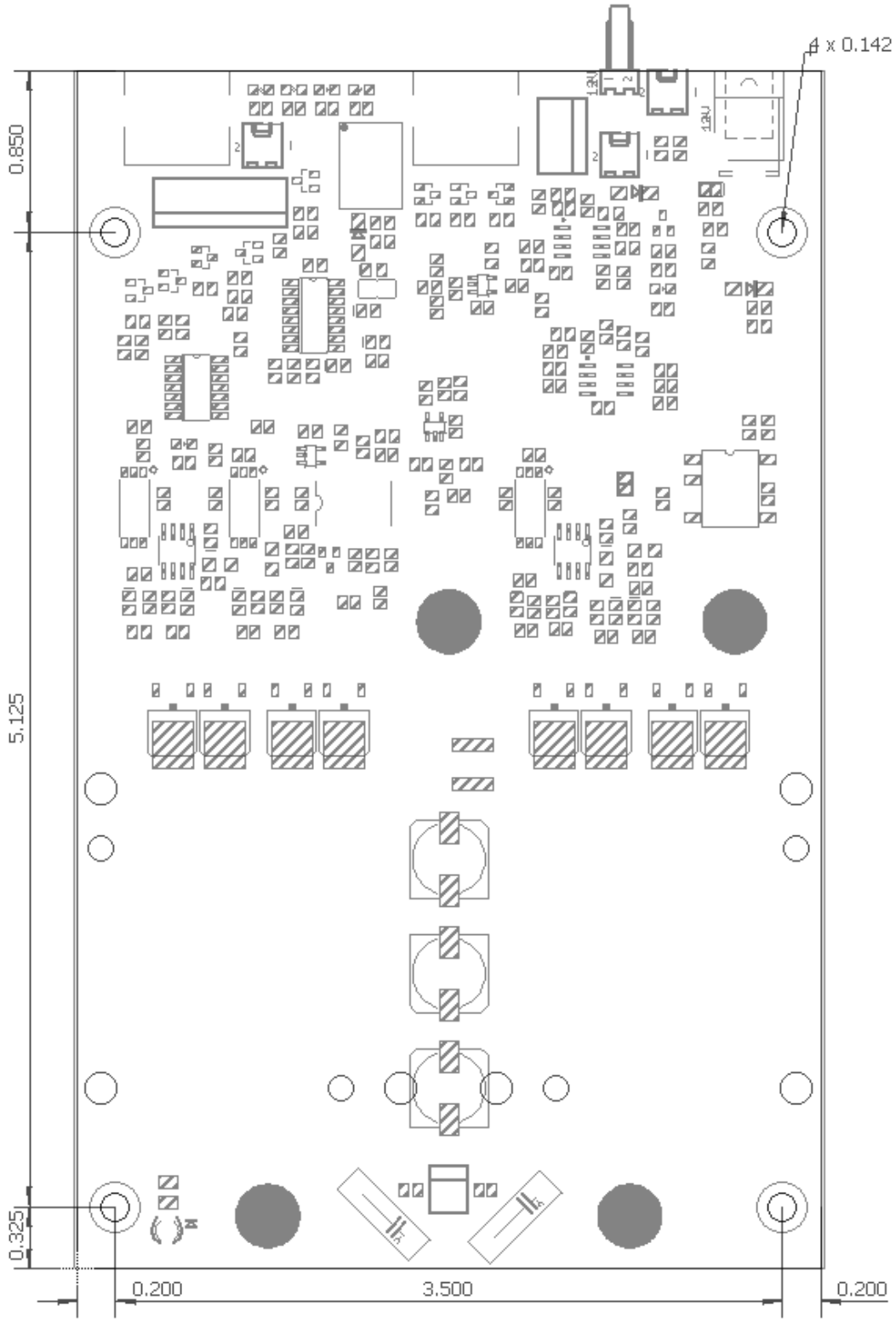
Pin Number		Signal Name
1		Analog Ground
2		Temperature
3		NC
4		NC
5		Voltage Monitor
6		Current Monitor

miniDIN, 8 Pin

Pin Number		Signal Name	Signal Type
1		Digital Ground	
2		NC	
3		5V	Output
4		Fault RESET	Input (Active Low)
5		Phase B	Input
6		Phase A	Input
7		STATUS	Output
8		ENABLE	Input




AL
AH
A
BL
BH
B
35V
50A
SPI-DCI-35V50A-NI-1.1
Design by W. Mefford
1/9/2020
DC-
DC+
R51
R52
CY1
CY2
R12



All dimensions in inches

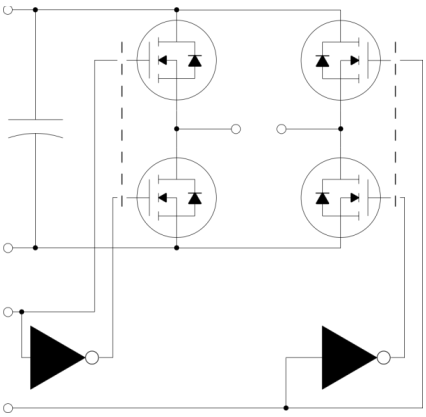
Application Information

1. Architecture

The SPI-DCI-35V-50A-NI-NF-1 is broadly split into two sections: the power section that includes the H-bridge and the control section that allows for easy interfacing with the switches in the H-bridge.

The H-bridge is a conventional topology composed of four power switches, but each of these ideal switches is constructed by paralleling two MOSFETs, giving a total of eight switching devices. Each MOSFET also has an integrated free-wheeling diode (the body diode), though this is typically activated only on the order of microseconds during switching events since the input logic forces a switch in each phase to be on as long as the system is enabled.

The MOSFETs are driven by two dual gate-drive circuits, each powered either by the 12V DC power supply or from a boot-strap circuit. The boot-strap circuits impose a maximum refresh time for the lower switches of roughly 2.5ms to allow the high side boot-strap capacitors to maintain charge. Without refreshing the boot-strap circuit, a high-side transistor in the on state will gradually loose charge and turn off unexpectedly, tri-stating the leg.



The DC bus is supported by six electrolytic capacitors totaling 1320µF which is suitable to control the ripple of many loads, but also mitigates spikes on the DC bus due to switching. Additional capacitance may need to be added externally for certain loads or sources to reduce DC bus ripple and capacitor heating. The DC bus also features a red LED to alert the user to the presence of a voltage as well as slowly discharge the capacitor bank. This results in an effective resistance of roughly 6.2kΩ across the DC bus.

The H-bridge is monitored by three sensors: the heatsink is monitored by an NTC thermistor, the DC bus voltage is monitored through a voltage divider, and the current is monitored through a Hall Effect sensor on Phase A. These analog signals are provided to the user and are also used to trigger a shut-down of the inverter should their values go too high.

The low-power section interfaces with the gate drivers through filters and buffers to make interfacing simple. An external 12V supply (provided) is required to operate the low-power section, though it is regulated down to 5V to power the low-voltage section and provide an auxiliary supply to the user. The logic inputs accept both 5V and 3.3V signals and have 100kΩ input impedances.

2. H-Bridge Control

The SPI-DCI-35V-50A-NI-NF-1 has four digital control inputs: Phase A, Phase B, ENABLE, and RESET. Each input except Reset has a 100kΩ resistor to ground followed by an LC filter and a CMOS buffer.

T The two switches constituting a phase are controlled with one signal and dead-time is automatically inserted for the user in the gate drivers. Essentially, the two-phase controls behave as extensions of the controlling device: when the control signal is high, the phase terminal is connected to DC+, when the signal is low, the phase terminal is connected to DC-.

The ENABLE signal is logically "ANDed" with the two phase controls so that when high, the two control signals control the MOSFETs as described above, and when low, all of the MOSFETs are off, regardless of the phase controls' states. Setting the ENABLE signal to low, or disabling the inverter, can also be thought of as "tri-stating" the H-bridge. It should be noted that if the load is inductive and carrying a current, the free-wheeling diodes will continue to conduct in an uncontrolled fashion despite the H-bridge being disabled, passing energy to the DC bus.

In the event a fault condition is detected, the inverter will be latched in the disabled state. To continue operating the inverter, the RESET input must be toggled. The RESET input is active low and should normally be in the high state. Unlike the other controls, RESET has a 10kΩ pull-up resistor to the 5V rail at the input. If the RESET pin is held low while the inverter is switching, fault conditions will cause the H-bridge to only be momentarily disabled or to ignore certain faults all together. While this can be useful if faults are being falsely reported, this technique is highly discouraged.

In addition to the four digital inputs, there is also the digital output STATUS which reports to the user's controller the operational state of the H-bridge. A high state indicates that the H-bridge is operational; a low state indicates that the H-bridge is presently latched in the disabled state due to a detected fault.

ENABLE	Phase A/B In	Terminal A/B
Low	Low	Tri-State
Low	High	Tri-State
High	Low	Low
High	High	High

3. Monitors and Faults

There are three analog monitors available to the user: DC bus voltage, A phase current, and heatsink temperature. Each of these is buffered, utilizing a 0-5V range. The DC bus monitor is proportional to the DC bus voltage where the relationship is $12.5V_{bus}/V_{mon}$. It has the relatively low bandwidth of 150 Hz limiting its usefulness in feedback schemes. The current monitor also has a proportional relationship, 33.3A/V, but is offset by 2.5V to accommodate the bidirectional nature of the possible currents. It has a much higher bandwidth of 40kHz, dictated by passive filter. The temperature monitor does not have a straightforward relationship to the measured temperature. Instead, a table of temperatures and corresponding voltages is provided in the data above. A straight-line approximation between those values should be accurate enough for most applications. It may also be the case that switching noise is induced on the monitor lines on their way to the controller so it is recommended that

filtering be added at the monitors' entrance to the user's controller.

Each of these monitors is also used by the H-bridge to determine if a fault is present. In the event a fault condition is triggered, the H-bridge will be disabled in an attempt to spare the inverter and the equipment it is connected to. This disabled state is latched and requires a pulsed low RESET signal to continue operating the inverter. There is also a corresponding LED lit on the front panel to indicate the nature of the fault. However, simply halting active switching is not always desirable in the event of a fault or malfunction so the user may want to implement his or her own shut-down routine or limiting function triggered by values lower than those used by the H-bridge. For example, many loads can store a great deal of energy, that during a shut-down of the inverter, can cause the activation of the free-wheeling diodes, dumping the stored energy onto the DC bus. Enough energy could cause the bus voltage to rise above the rated voltage of the MOSFETs so that despite our efforts to save the system, we will have instead had a hand in destroying it. There are of course several ways to mitigate this particular scenario, but the point being that consideration should be given to the fault conditions used by the H-bridge and the effects the inverter's shut-down will have in those circumstances.

There are three conditions which lead to the H-bridge being disabled: a current in either direction exceeding 50A, a bus voltage exceeding 50V, and a heatsink temperature exceeding 55°C. If damage is suspected as the result of one of these conditions being met, the entire system should be powered down and the resistance of the MOSFETs in their powered down state checked. Testing from each phase terminal to each DC rail with the inverter completely powered down should present a resistance on the order of 1MΩ. A damaged MOSFET will instead present a resistance on the order of tenths of an Ohm.

4. Heat and Cooling

The SPI-DCI-35V-50A-NI-NF-1 is a passively air-cooled system as shipped, though it is possible to cool the module with external fans, improving its performance and extending its advertised power range. An NTC thermistor is thermally connected to the AH MOSFETs and the resulting signal provided to the user. A table is provided above relating the resulting voltages and the corresponding temperatures.

In general the cooler the environment, the more effective the heat sinks will be. To estimate the temperature of the MOSFETs (measured at the package), refer to the previously provided graph of collected data. If the ambient temperature is known, the operating curves can be estimated by adding the difference between the ambient temperature and 25°C, effectively shifting all of the curves up or down.

5. Paralleling Phases

For applications where only a half-bridge or one phase-leg is required, it will likely be advantageous to parallel the two phases available in the H-bridge, reducing losses. To parallel the two, simply run a cable from one phase output to the other and route the same control signal as A Phase to the B phase control input. They must have identical control signals to avoid a shoot-through condition from occurring.

6. DC Bus Capacitor Bank

The DC Bus has integrated into it a 1320µF electrolytic capacitor bank rated at 50V, the same as the MOSFETs. For many applications, this will be a sufficiently sized capacitance, but often ripple voltage or ripple current caused by either the source (e.g. passive rectifier) or load will require additional capacitance. Additionally, many loads can store a great deal of energy that can be transferred to the DC bus periodically or while halting the load. The voltage rise due to this energy transfer could exceed the maximum voltage of the DC bus, destroying the MOSFETs, which will undoubtedly protect the capacitors. Externally adding capacitance to the DC bus is a relatively simple task so long as one knows how to appropriately size a capacitor bank, the only precaution being that the conductors between the two should be as low impedance (short) as possible.

Another important design feature—or lack thereof—to keep in mind is that there is no capacitor charging circuit. The bus voltage will need to be ramped in some fashion if a DC source is connected to it. Abruptly connecting a voltage to the capacitor bank will cause an in-rush current that could destroy or damage the capacitors, destroy or damage the voltage source, or at the very least, trigger safety measures "upstream".

7. Grounding

Both the control and power portions of the PCB share the same reference. On the power side, this is referred to as DC- and on the control side this is referred to as Gnd, though both are connected by thick traces that cut across a conductive barrier intended to separate the sides. Additionally, the shield of the control cable is connected through a trace to Gnd and a two-pin header is provided to easily connect to the cable's shield. Effectively, this interconnectedness makes the entire system referenced to the negative DC bus, which could require special care. For example, if a conventional passive rectifier is used to provide DC power to the inverter, the negative rail will not be at ground potential unless an isolation transformer is used and a connection to ground deliberately made. The absence of either of these conditions will either lead to a floating DC bus, or a short across the rectifier, potentially destroying the diode and the high current taking an unexpected path through the controller.

Incomplete Items:
Propagation delay
Monitor bandwidths
Temperature relationship
Molex connectors